

REMARKS

Claims 1-12 are pending in the present application. Claims 1, 5, 6, 7, 11, and 12 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 5-6 and 11-12 stand rejected under 35 U.S.C. 112, second paragraph, for reasons stated in the Office Action. The claims are amended above in a manner that is believed to overcome the rejections. With regard to the rejection of claims 6 and 12, to clarify, in amended claims 6 and 12, the "first PMOS transistor" corresponds to transistor P7 of FIG. 3, the "second PMOS transistor" corresponds to transistor P6 of FIG. 3, and the "third PMOS transistor" corresponds to transistor P8 of FIG. 3. The claims are amended above to address the issues raised with regard to the "third PMOS transistor" (formerly the "eighth PMOS transistor"). Entry of the amendments and removal of the rejections are respectfully requested.

Applicant notes, with appreciation, that the Office Action indicates at paragraph 5 that Claims 3-4 and 8-10 would be allowable if rewritten in independent form. The Applicant wishes to defer submission of these claims, pending consideration of the present amendment.

Claims 1, 2 and 7 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jung (U.S. 6,529,060). Reconsideration of the rejection and allowance of claims 1-12 are respectfully requested.

The present invention as claimed in independent claim 1 is directed to an input buffer. The input buffer includes a single pull-up transistor connected between a power supply voltage and an input pad. The pull-up transistor has a gate to which a control voltage is applied and a substrate to which a floating well voltage is applied. A transmission transistor has a gate to which the power supply voltage is applied and a substrate connected to a ground voltage. The transmission transistor transmits at an output terminal a signal applied to the input pad. A buffer includes an input terminal coupled directly and exclusively to the output terminal of the

transmission transistor. The buffer generates an input signal by buffering the signal transmitted by the transmission transistor. A controller generates the voltage of the signal applied to the input pad as the control voltage and the floating well voltage when a high voltage is applied to the input pad. The controller further generates the ground voltage as the control voltage and the power supply voltage as the floating well voltage in the case where a voltage less than the high voltage is applied to the input pad.

The present invention as claimed in independent claim 7 is directed to an input buffer. The input buffer includes a single pull-up transistor connected between a power supply voltage and an input pad. A transmission transistor has a gate to which the power supply voltage is applied and a substrate connected to a ground voltage. The transmission transistor transmits at an output terminal a signal applied to the input pad. A buffer includes an input terminal coupled directly and exclusively to the output terminal of the transmission transistor. The buffer generates an input signal by buffering the signal transmitted by the transmission transistor. A controller turns off the pull-up transistor when a high voltage is applied to the input pad, and turns on the pull-up transistor in the case where a voltage less than the high voltage is applied to the input pad.

In the present invention as claimed in independent claims 1 and 7, an “input buffer” includes “a single pull-up transistor” as claimed in claims 1 and 7. Further, a “controller” turns “off the single pull-up transistor when a high voltage is applied to the input pad”, and turns “on the single pull-up transistor in the case where a voltage less than the high voltage is applied to the input pad”, as claimed in claim 7. Thus, the present invention as claimed in claims 1 and 7 is directed to an input buffer that includes only a “single” pull-up transistor that receives the control voltage from the controller (claim 1) or that is turned on and off in response to the controller (claim 7).

In addition , in the present invention as claimed in claims 1 and 7, the “buffer” of the “input buffer” has “an input terminal coupled directly and exclusively to the output terminal of

the transmission transistor". This feature of the present invention is illustrated at least at FIG. 2 and FIG. 3 which illustrate the output terminal of transmission transistor N2 coupled directly and exclusively to the input terminal of buffer BUF2.

In contrast, Jung includes a first PMOS "pull-up" transistor MP10, a second PMOS "pull-up" transistor MP12, an input pad 200, a transmission transistor MN10, and a controller 140, 120, 160. The controller controls both the first and the second PMOS transistors MP10, and MP12. When a voltage higher than the power supply is applied to the input pad, the first PMOS transistor MP10 is turned off and the second PMOS transistor MP12 is turned on. When a voltage lower than the power supply is applied to the input pad, the first PMOS transistor MP10 is turned on and the second PMOS transistor MP12 is turned off (Jung, column 4, lines 11-23). The first and second PMOS transistors MP10, MP12 operate complementary to each other, according to the voltage applied to the input pad. The controller controls the complementary operations of both the first and second PMOS transistors MP10, MP12.

It is submitted that Jung fails to teach or suggest the present invention as claimed in independent claims 1 and 7. In particular, Jung fails to teach or suggest an input buffer that includes a "single" pull-up transistor. Instead, the Jung embodiment includes dual pull-up transistors MP10 and MP12 that are responsive to dual control signals PU1 and PU2 generated by the signal generator 160. Thus, with respect to claim 7, Jung further fails to teach or suggest a "controller" that turns "off the single pull-up transistor when a high voltage is applied to the input pad", and turns "on the single pull-up transistor in the case where a voltage less than the high voltage is applied to the input pad". Instead, Jung teaches the controller turning on and off the dual pull-up transistors via dual control signals PU1, PU2.

In addition, it is submitted that Jung fails to teach or suggest the "buffer" of the "input buffer" having "an input terminal coupled directly and exclusively to the output terminal of the transmission transistor", as claimed in claim 1 and 7. Instead, in Jung, the input terminal of the "internal logic 300" is coupled to the output terminal of transistor MN10, and also the terminal of

the second pull-up transistor MP12 at node ND1.

Reconsideration of the rejections of claims 1 and 7 under 35 U.S.C. 102(e) as being anticipated by Jung is therefore respectfully requested. In view of the above, it is submitted that independent claims 1 and 7 are in condition for allowance, and such allowance is respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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